

IN THE CLAIMS:

1 1. (Currently Amended) An integrated circuit comprising:
2 a power supply I/O pad;
3 an I/O pad of a first type made of a deposited conductor, wherein the I/O pad of the first
4 first type is connected to a first point on an integrated circuit; and
5 a strip of deposited conductor substantially adjacent to the I/O pad of the first type,
6 wherein the strip of ~~disposed~~ deposited conductor is connected to a second point on the
7 integrated circuit, and wherein the I/O pad of the first type is narrower than the power supply I/O
8 pad so as to allow space for the strip.

1 2. (Previously Amended) The integrated circuit of claim 1, wherein the I/O pad of the first
2 type is selected from a group consisting of a data I/O pad and a multi-level voltage I/O pad.

1 3. (Original) The integrated circuit of claim 1, wherein the first point on the integrated
2 circuit is further connected to a circuitry.

1 4. (Original) The integrated circuit of claim 1, wherein the first point on the integrated
2 circuit is further connected to a power bus.

1 5. (Original) The integrated circuit of claim 1, wherein the second point on the integrated
2 circuit is further connected to a circuitry.

1 6. (Original) The integrated circuit of claim 1, wherein the second point on the integrated
2 circuit is further connected to a power bus.

1 7. (Original) The integrated circuit of claim 1, wherein the strip of conductor is connected to
2 a third point on the integrated circuit.

1 8. (Original) The integrated circuit of claim 7, wherein the second and third points on the
2 integrated circuit are connected to a circuitry.

- 1 9. (Original) The integrated circuit of claim 7, wherein the second and third points on the
2 integrated circuit are connected to a power bus.
- 1 10. (Previously Amended) The integrated circuit of claim 1, further comprising an I/O pad of
2 a second type made of a deposited conductor, wherein the I/O pad of the second type is
3 connected to a third point on the integrated circuit.
- 1 11. (Previously Amended) The integrated circuit of claim 10, wherein the I/O pad of the
2 second type is selected from a group consisting of a data I/O pad and a multi-level voltage I/O
3 pad.
- 1 12. (Original) The integrated circuit of claim 10, wherein the third point on the integrated circuit
2 is further connected to a circuitry.
- 1 13. (Original) The integrated circuit of claim 10, wherein the third point on the integrated circuit
2 is further connected to a power bus.
- 1 14. (Previously Amended) The integrated circuit of claim 10, wherein the strip of deposited
2 conductor is connected to a fourth point on the integrated circuit.
- 1 15. (Original) The integrated circuit of claim 14, wherein the second, third and fourth points on
2 the integrated circuit are connected to a circuitry.
- 1 16. (Original) The integrated circuit of claim 14, wherein the second, third and fourth points on
2 the integrated circuit are connected to a power bus.
- 1 17. (Original) The integrated circuit of claim 1, wherein the I/O pad of the first type provides
2 power to a core circuitry.
- 1 18. (Currently Amended) The integrated circuit of claims 4, ~~6, 9, 13 or 16~~ wherein the power

2 bus is configured as an intersecting grid of a deposited conductor.

1 19. (Original) The integrated circuit of claim 18, wherein the integrated circuit is comprised of
2 multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited
3 on different layers.

1 20. (Original) The integrated circuit of claim 19, wherein the power bus exists at a lowest layer.

1 21. (Original) The integrated circuit of claim 19, wherein the power bus exists at a
2 second to lowest layer.

1 22. (Previously Amended) An integrated circuit comprising:
2 a power supply I/O pad made of a deposited conductor;
3 a power bus connected to the power supply I/O pad;
4 a data I/O pad made of a deposited conductor;
5 circuitry connected to the data I/O pad; and
6 a strip of deposited conductor substantially adjacent to the data I/O pad wherein the strip
7 of deposited conductor is connected to multiple points on the power bus, and wherein the
8 data I/O pad is narrower than the power supply I/O pad so as to allow space for the strip.

1 23. (Original) The integrated circuit of claim 22, wherein the power bus provides
2 power to a core circuitry.

1 24. (Original) The integrated circuit of claim 22, wherein the power bus is configured as an
2 intersecting grid of a deposited conductor.

1 25. (Original) The integrated circuit of claim 22, wherein the integrated circuit is comprised
2 of multiple metal layers, and wherein the power supply I/O pad and the power bus are
3 deposited on different layers.

1 26. (Previously Amended) The integrated circuit of claim 25, wherein the power bus exists at the

2 lowest layer.

1 27. (Original) The integrated circuit of claim 25, wherein the power bus exists at the
2 second to the lowest layer.

1 28. (Previously Amended) An integrated circuit comprising:
2 a power supply I/O pad made of a deposited conductor;
3 a power bus connected to the power supply I/O pad;
4 a multi-level voltage I/O pad made of a deposited conductor;
5 circuitry connected to the multi-level voltage I/O pad; and
6 a strip of deposited conductor substantially adjacent to the multi-level voltage I/O pad
7 wherein the strip of deposited conductor is connected to multiple points on the power bus, and
8 wherein the multi-level voltage I/O pad is narrower than the power supply I/O pad so as to allow
9 space for the strip.

1 29. (Original) The integrated circuit of claim 28, wherein the power bus provides
2 power to a core circuitry.

1 30. (Original) The integrated circuit of claim 28, wherein the power bus is configured as
2 an intersecting grid of a deposited conductor.

1 31. (Original) The integrated circuit of claim 28, wherein the integrated circuit is
2 comprised of multiple metal layers, and wherein the power supply I/O pad and the power
3 bus are deposited on different layers.

1 32. (Currently Amended) The integrated circuit of claim 31, wherein the power bus
2 bus exists at the lowest layer.

1 33. (Original) The integrated circuit of claim 31, wherein the power bus exists at the
2 second to the lowest layer.

1 34. (Previously Amended) An integrated circuit comprising:
2 a positive power supply I/O pad made of a deposited conductor;
3 a positive power bus connected to the positive power supply I/O pad;
4 a negative power supply I/O pad made of a deposited conductor;
5 a negative power bus connected to the negative power supply I/O pad;
6 a data or multi-level voltage I/O pad made of a deposited conductor;
7 circuitry connected to the data or multi-level voltage I/O pad;
8 a first strip of deposited conductor substantially adjacent to the data or multi-level voltage
9 I/O pad, wherein the strip of deposited conductor is connected to multiple points on the positive
10 power bus; and
11 a second strip of deposited conductor substantially adjacent to the data or multi-level
12 voltage I/O pad, wherein the second strip of deposited conductor is connected to multiple points
13 on the negative power bus, and wherein the data or multi-level voltage I/O pad is narrower than
14 the power supply I/O pad so as to allow space for the first and second strip.

1 35. (Original) The integrated circuit of claim 34, wherein the power buses provide
2 positive and negative power to a core circuitry.

1 36. (Original) The integrated circuit of claim 34, wherein the power buses are
2 configured as intersecting grids of a deposited conductor.

1 37. (Original) The integrated circuit of claim 34, wherein the integrated circuit is comprised
2 of multiple metal layers, and wherein the positive and negative power buses are deposited
3 on third and fourth layers, respectively.

1 38. (Original) The integrated circuit of claim 34, wherein the integrated circuit is comprised
2 of multiple metal layers, and wherein the positive and negative power supply I/O pads are
3 deposited on a first and second layer, respectively.

1 39. (Original) The integrated circuit of claim 38, wherein the first and second layers are the same
2 layer.

1 40. (Original) The integrated circuit of claim 38, wherein the negative power bus exists at
2 the lowest layer.

1 41. (Original) The integrated circuit of claim 38, wherein the positive power bus exists
2 at the lowest layer.

1 42. (Original) The integrated circuit of claim 38, wherein the negative power bus exists
2 at the second lowest layer.

1 43. (Original) The integrated circuit of claim 38, wherein the negative and positive
2 power buses are further deposited on a fifth and sixth layer.

1 44. (Original) The integrated circuit of claim 38, wherein the positive power bus exists at
2 the second lowest layer.

1 45. (Original) The integrated circuit of claim 44, wherein the negative power bus exists
2 at the third lowest layer.

1 46. (Original) The integrated circuit of claim 44, wherein the positive power bus exists
2 at the third lowest layer.

1 47. (Original) The integrated circuit of claim 44, wherein the negative power bus exists
2 at the fourth lowest layer.

1 48. (Original) The integrated circuit of claim 44, wherein the positive power bus exists at the
2 fourth lowest layer.

1 49. (New) The integrated circuit of claims 6, wherein the power bus is configured as an
2 intersecting grid of a deposited conductor.

1 50. (New) The integrated circuit of claims 9, wherein the power bus is configured as an
2 intersecting grid of a deposited conductor.

1 51. (New) The integrated circuit of claims 13, wherein the power bus is configured as an
2 intersecting grid of a deposited conductor.

1 52. (New) The integrated circuit of claims 16, wherein the power bus is configured as an
2 intersecting grid of a deposited conductor.